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Assistant Commissioner for Patents Box Patent Applications Washington D.C. 20231

Attorney Docket No.10.249.216 (must include alphanumeric codes if no inventors named)

UTILITY PATENT APPLICATION TRANSMITTAL (new nonprovisional applications under 37 CFR 1.53(b))

Transmitted herewith for filing is the patent application of:

INVENTOR(S): In-Kyeong YOO

TITLE: FERROELECTRIC EMITTER

In connection with this application, the following are enclosed:

APPLICATION ELEMENTS:

<u>xx</u> Specification - <u>10</u> TOTAL PAGES

(preferred arrangement:)

- -Descriptive Title of the Invention
- -Cross Reference to Related Applications
- -Statement Regard Fed sponsored R&D
- -Reference to Microfiche Appendix
- -Background of the Invention
- -Brief Summary of the Invention
- -Brief Description of the Drawings (if filed)
- -Detailed Description
- -Claim(s)
- -Abstract of the Disclosure

XX Drawings - Total Sheets 5

XX Declaration and Power of Attorney - Total Sheets 2

- XX Newly executed (original or copy)
- ____ Copy from a prior application (37 CFR 1.63(d))
 - (relates to continuation/divisional boxes completed) NOTE: Box below
- DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

<u>Incorporation By Reference</u> (useable if copy of prior application Declaration being submitted)

The entire disclosure of the prior application, from which a COPY of the oath or declaration is supplied as noted above, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

____ Microfiche Computer Program (Appendix)

Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)

- ____ Computer Readable Copy
 - Paper Copy (identical to computer copy)
 - ___Statement verifying identify of above copies

Utility Patent Application Transmittal Attorney Docket No. 10.249.216
Page 2

ACCOMPANYING APPLICATION PARTS
XX Assignment Papers (cover sheet & document(s)) 37 CFR 3.73(b) Statement (when there is an assignee) English Translation Document (if applicable) Information Disclosure Statement(IDS) with PTO-1449 Copies of IDS Citations Preliminary Amendment XX Return Receipt Postcard (MPEP 503) Small Entity Statement(s) Statement file in prior application, status still proper and desired Certified Copy of Priority Document(s) with Claim of Priority
If a <u>CONTINUING APPLICATION</u> , check appropriate box and supply the requisite information: Continuation Divisional Continuation-in-part (CIP) of prior application Serial No
Amend the specification by inserting before the first line the following sentence:This application is a continuation, divisional or continuation-in-part of application Serial No filed
CORRESPONDENCE ADDRESS: KILE, MCINTYRE, HARBIN & LEE- address noted above. Telephone: (202) 639-1260 Fax Number: (202) 639-1299

FEE CALCULATIONS: (Small entity fees indicated in parentheses.)

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	(1) For	(2) Number Filed	(3) Number Extra	(4) Rate	(5) Basic Fee \$690 (\$345)
	Total Claims	7 - 20 =	0	x \$18 (x \$9)	0.00
	Independent Claims	2 - 3 =	0	x \$78 (x \$39)	0.00
	Multiple Dependent Claims			\$260 (\$130)	0.00
	Assignment Recording Fee per property			\$40	40.00
				TOTAL FEE:	730.00

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A check in the amount of the above TOTAL FEE is attached. If payment is enclosed, this amount is believed to be correct; however, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 11-0853.

Respectfully submitted,

Date: September 20, 2000

Eugene M. Lee Reg. No. 32,039

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FERROELECTRIC EMITTER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a ferroelectric emitter. More specifically, the present invention relates to a ferroelectric multi-layered emitter used in a semiconductor lithography process.

2. Description of the Related Art

Ferroelectric emission by switching allows for a simple process in electron emission lithography. In the past, electron emission suitable for lithography has been obtained by switching an emitter in a magnetic field. However, a conventional ferroelectric emitter cannot guarantee electron emission where the gap between two electrodes is too wide or too narrow for switching.

For example, in the conventional ferroelectric emitter, if the gap between two electrodes is too wide an electric field cannot reach the center portion of the ferroelectric emitter. Thus a switching effect does not occur in a ferroelectric region. If, on the other hand, the gap between the two electrodes, or a gap of a mask pattern, is too narrow, then the mask pattern formed on a ferroelectric layer in a ferroelectric emitter absorbs electrons during electron emission, so that electrons flow through the patterned mask. Moreover, an isolated pattern, such as a doughnut shape, cannot be switched because the two electrodes are not connected to each other.

In contrast to ferroelectric switching, pyroelectric emission can provide a uniform emission of electrons regardless of the characteristics of a gap of a mask pattern. Pyroelectricity refers to the production of polarization changes by temperature variations. Due to such properties, when a material is subjected to a temperature change, the magnitude of a spontaneous polarization changes to affect bound charges, so that a current flows between the top and bottom electrodes.

If an emitter is heated and this process occurs in a vacuum, then bound charges, which are electrons screening on the surface of the emitter, are released in a vacuum, which is called pyroelectric emission. In this case, uniform emission is allowed regardless of a gap distance. Furthermore, pyroelectric emission enables uniform electron emission in an isolated pattern such as a doughnut pattern. Although it facilitates electron emission, pyroelectric emission has several

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disadvantages. One of the disadvantages is the requirement the restriction of repoling an emitter or heating an emitter above the Curie temperature for re-emission.

SUMMARY OF THE INVENTION

A feature of the present invention is to provide a ferroelectric emitter that guarantees uniform emission of electrons from both wide and narrow gaps of a mask pattern and in an isolated pattern such as a doughnut shape for ferroelectric switching emission lithography while eliminating a need to heat an emitter above the Curie temperature for re-emission.

The present invention provides a ferroelectric emitter including: a lower electrode; a ferroelectric layer, having a top surface with two end portions, which overlies the lower electrode; an insertion electrode formed on a region excluding the two end portions of the top surface of the ferroelectric layer; a dielectric layer, having a top surface with two end portions, having a predetermined pattern and formed along the top surface of the ferroelectric layer and the insertion electrode; and a dummy upper electrode formed on one side of the dielectric layer opposite the ferroelectric layer.

In a preferred embodiment of the present invention, the predetermined pattern is formed in the top surface of the dielectric layer excluding the two end portions thereof, and the dummy upper electrode is easily separable from the dielectric layer. The dummy upper electrode is formed on a region excluding the patterned portion of the dielectric layer.

The present invention also provides a ferroelectric emitter including: a lower electrode; a ferroelectric layer, having a top surface with two end portions, which overlies the lower electrode; an insertion electrode formed on a region excluding the two end portions of the top surface of the ferroelectric layer; a first dielectric layer, having projected side edges, is formed along the top surface of the ferroelectric layer and the insertion electrode; a second dielectric layer formed along the top surface of the first dielectric layer excluding the projected side edges; and a dummy upper electrode formed on one projected side of the first dielectric layer.

In another preferred embodiment of the present invention, the dielectric constant of the first dielectric layer is higher than the dielectric constant of the second dielectric layer, and the dummy upper electrode is readily separable from the first dielectric layer.

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BRIEF DESCRIPTION OF THE DRAWINGS

The above-described feature and advantages of the present invention will become more apparent by describing in detail preferred embodiments of the present invention with reference to the attached drawings in which:

- FIG. 1 is a cross-sectional view showing the structure of a ferroelectric emitter according to a preferred embodiment of present invention;
- FIG. 2A is a cross-sectional view showing an initialization step in which a constant voltage is applied to the ferroelectric emitter for switching emission lithography according to the present invention, to which a dummy upper electrode is attached:
- FIG. 2B is a cross-sectional view showing a screening step in which the dummy upper electrode is separated from the ferroelectric emitter for switching emission lithography subjected to the initialization step shown in FIG. 2A;
- FIG. 2C is a cross-sectional view showing an emission step in which a negative voltage is applied to the ferroelectric emitter for switching emission lithography, which is subjected to the screening step shown in FIG. 2B, and to which the dummy upper electrode is attached;
- FIG. 3A is a cross-sectional view showing an initialization step in which a constant voltage is applied to a ferroelectric emitter for pyroelectric emission lithography according to the present invention, to which a dummy upper electrode is attached;
- FIG. 3B is a cross-sectional view showing a screening step in which the dummy upper electrode is separated from the ferroelectric emitter for pyroelectric emission lithography subjected to the initialization step shown in FIG. 3A;
- FIG. 3C is a cross-sectional view showing an emission step in which a negative voltage is applied to the ferroelectric emitter for pyroelectric emission lithography, which is subjected to the screening step shown in FIG. 3B, and to which the dummy upper electrode is attached; and
- FIG. 4 is a cross-sectional view showing the structure of a ferroelectric emitter according to another preferred embodiment of present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to FIG. 1, a ferroelectric emitter according to a preferred embodiment of the present invention includes an insertion electrode 12 formed on a top surface of a ferroelectric layer 11. A dielectric layer 13 having a predetermined

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pattern is formed along the top surface of the ferroelectric layer 11 and the insertion electrode 12. The ferroelectric layer and the dielectric layer both having a top surface with two end portions. Thus, a top and two sides of the insertion electrode 12 are surrounded by the dielectric layer 13. Since the dielectric layer 13 is formed along the top surface of the ferroelectric layer 11 and the insertion electrode, a portion formed along the top surface of the ferroelectric layer 11 is thicker than a portion formed along a top surface of the insertion electrode 12. The predetermined pattern is formed at the top surface of the dielectric layer 13, over the insertion electrode 12.

A dummy upper electrode 14 is provided on the dielectric layer 13. The dummy upper electrode 14 is easily separable during the operation of the ferroelectric emitter according to the present invention. The dummy upper electrode 14 is formed along the top surface of an unpatterned portion of the dielectric layer 13. A lower electrode 15 underlies the ferroelectric layer 11, and the lower electrode 15 applies an external charge when operating the ferroelectric emitter according to the present invention. The insertion electrode 12 overlying the ferroelectric layer 11 is positioned between the lower electrode 15 and the dummy upper electrode 14. When an electric field is applied, the insertion electrode 12 serves to polarize the ferroelectric layer 11 around a center region thereof. Furthermore, the insertion electrode 12 serves to collect electrical charges between patterns of the dielectric layer 13, when separating the dummy upper electrode 14.

In FIG. 1, a collector 16 is provided outside the ferroelectric emitter according to the present invention, and electrons emitted from the dielectric layer 13 during the operation of the emitter reach the collector 16.

Referring now to FIG. 2A, an initialization step for electron emission will be described. First, a constant voltage is applied between the lower electrode 15 and the dummy upper electrode 14. Thus, the ferroelectric layer 11 becomes polarized 21 in order to collect positive bound charges in the lower electrode 15 and collect negative bound charges in the dummy upper electrode 14. In an initialization step, an electric field is induced between the dummy upper electrode 14 and the insertion electrode 12. An electric field is also induced between the insertion electrode 12 and the lower electrode 15. Additionally, the ferroelectric layer 11 becomes polarized within a region corresponding to the area of the insertion electrode 12.

Referring to FIG. 2B, a screening step that follows the initialization step will now be described. If the dummy upper electrode 14 formed along the top surface of

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the patterned dielectric layer 13 is separated from the dielectric layer 13, the negative bound charges within the dummy upper electrode 14 abruptly disappear from the emitter. To compensate for this, electrons 22 in a vacuum collect at the patterned portion of the dielectric layer 13. In this case, since more electrons are collected at a thin portion of the dielectric layer than at a thick portion thereof, electrons are collected around the center portion of the dielectric layer 13, which is patterned. As a spontaneous polarization is larger and a dielectric layer is thinner, more electrons 22 are collected.

An emission lithography process by switching and a pyroelectric emission lithography process are substantially the same until the screening step is performed. However, when the electron emission step is entered, the processes differ. Referring now to FIG. 2C, during an emission step for switching emission lithography, a negative voltage is applied between the dummy upper electrode 14 and the lower electrode 15, which is unlike the initialization step. Thus, positive bound charges are collected in the dummy upper electrode 14 and negative bound charges are collected in the lower electrode 15, so that polarization 23 occurs in the opposite direction to the polarization 21 produced in the initialization step. In this case, when positive charges are bound in the dummy upper electrode 14 and negative charges are bound in the lower electrode 15, electrons 24 collecting at the top surface of the dielectric layer 13 are released to move toward a collector 16. Thus, electrons 24 are emitted in this way to perform emission lithography by switching.

Next, referring to FIG. 3A, during an initialization step for electron emission in pyroelectric emission lithography, a constant voltage is applied between the lower electrode 15 and the dummy upper electrode 14. Put another way, in order to collect positive bound charges in the lower electrode 15 and negative bound charges in the dummy upper electrode 14, the ferroelectric layer 11 becomes polarized 31. During the initialization step, an electric field is induced between the dummy upper electrode 14 and insertion electrode 12. Another electric field is induced between the insertion electrode 12 and the lower electrode 15. Additionally, the ferroelectric layer 11 becomes polarized within a region corresponding to the area of the insertion electrode 12.

Referring to FIG. 3B, during a screening step following the initialization step, the dummy upper electrode overlying a patterned dielectric layer 13 is separated from the dielectric layer 13. In this case, due to separation of the dummy upper

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electrode, the negative bound charges within the dummy upper electrode abruptly disappear from the emitter. To compensate for this, electrons 32 in a vacuum collect at the patterned top surface of the dielectric layer 13. In this case, since more electrons collect at a thin portion of the dielectric layer 13 than at a thick portion thereof, electrons gather together around a center portion that is patterned. As the magnitude of spontaneous polarization is larger and a dielectric layer is thinner, more electrons 32 are collected. A pyroelectric emission lithography process proceeds in the same manner as the emission lithography process by switching in the initialization and the screening steps, but the two methods differ in an emission step. The emission lithography technique by switching adopts a way of applying a negative voltage, unlike the initialization step, while a pyroelectric emission lithography technique adopts a way of applying heat to the ferroelectric emitter.

Referring to FIG. 3C, a pyroelectric emission lithography process according to the present invention will now be described. After going through the switching step, a ferroelectric layer 11 of the emitter is heated using an external heat source. The external heat source may be a heater, laser or infrared rays. When subjected to a heating step, the temperature of the ferroelectric layer 11 of the emitter goes up, reducing polarization 33. In this case, electrons 34 are emitted from the dielectric layer 13 in proportion to the reduction of polarization ,to the collector 16. Through this process, electrons can be emitted by performing a heating step instead of applying a voltage in emission lithography by switching.

A ferroelectric emitter according to another embodiment of the invention will now be described with reference to FIG. 4. The ferroelectric emitter of FIG. 4 is different from the ferroelectric emitter of FIG. 1 in that the material of the patterned portion (second dielectric layer) differs from the material of a first dielectric layer.

An insertion electrode 42 is formed along a center portion of a top surface of a ferroelectric layer 41. Along the top surface of the ferroelectric layer 41 and the insertion electrode 42 is formed a first dielectric layer 43, the edges of which are projected. Thus, a top surface and two sides of the insertion electrode 42 are surrounded by the first dielectric layer 43. The first dielectric layer 43 is formed along the top surface of the ferroelectric layer 41 and the insertion electrode 42. Thus, a portion overlying the ferroelectric layer is thicker than a portion overlying the insertion electrode 42. A second dielectric layer 44 having a predetermined pattern is formed on a portion excluding the projected edges of the first dielectric layer 43. A lower electrode 46 underlies the ferroelectric layer 41.

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The dielectric constant of the first dielectric layer 43 is different from that of the second dielectric layer 44. In the present invention, it is preferable that the dielectric constant of the former is higher than the dielectric constant of the latter. A dummy upper electrode 45 is formed on one projected side of the first dielectric layer 43. The dummy upper electrode 45 is readily detachable when operating the ferroelectric emitter according to another embodiment. The operating method of the ferroelectric emitter of FIG. 4 is the same as that of the ferroelectric emitter of FIG. 1. As shown in FIGS. 2A-3C, electron emission by switching and pyroelectric electron emission may be carried out in the same manner.

In the screening step, electrons are collected between patterns of the second dielectric layer 44, which is formed along the top surface, excluding the projected edges, of the first dielectric layer 43. The electrons are emitted during electron emission by switching or pyroelectric emission.

The present invention guarantees uniform emission of electrons from a wide or narrow region and in an isolated pattern such as a doughnut shape for ferroelectric emission lithography, while facilitating re-poling in pyroelectric emission. Accordingly, the present invention provides a ferroelectric emitter having many applications.

What is claimed is:

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a lower electrode;

a ferroelectric layer, having a top surface with two end portions, overlies the lower electrode;

an insertion electrode formed on a region excluding the two end portions of the top surface of the ferroelectric layer;

a dielectric layer having a predetermined pattern is formed along the top surface of the ferroelectric layer and the insertion electrode; and

a dummy upper electrode formed on a side of the dielectric layer opposite the ferroelectric layer.

- 2. The ferroelectric emitter as claimed in claim 1, wherein the dielectric layer has a top surface with two end portions and the predetermined pattern is formed along the top surface of the dielectric layer excluding the two end portions.
- 3. The ferroelectric emitter as claimed in claim 1, wherein the dummy upper electrode is easily separable from the dielectric layer.
- 4. The ferroelectric emitter as claimed in claim 1, wherein the dummy upper electrode is formed on a region of the dielectric layer excluding the patterned portion thereof.
 - 5. A ferroelectric emitter comprising:
 - a lower electrode;
- a ferroelectric layer, having a top surface with two end portions, overlies the lower electrode;

an insertion electrode formed on a region excluding the two end portions of the top surface of the ferroelectric layer;

a first dielectric layer having side edges and a top surface is formed along the top surface of the ferroelectric layer and the insertion electrode, the side edges being projected;

a second dielectric layer formed along the top surface of the first dielectric layer excluding the projected edges; and

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- a dummy upper electrode formed on one projected side of the first dielectric layer.
 - 6. The ferroelectric emitter as claimed in claim 5, wherein a dielectric constant of the first dielectric layer is higher than a dielectric constant of the second dielectric layer.
 - 7. The ferroelectric emitter as claimed in claim 5, wherein the dummy upper electrode is readily separable from the first dielectric layer.

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Abstract

A ferroelectric multi-layered emitter used in a semiconductor lithography process includes a lower electrode, a ferroelectric layer, having a top surface with two end portions, which overlies the lower electrode, an insertion electrode formed on a region excluding the two end portions of the top surface of the ferroelectric layer, a dielectric layer, having sides and a top surface with two end portions, which has a predetermined pattern and is formed along the top surface of the ferroelectric layer and the insertion electrode, and a dummy upper electrode formed on a side of the dielectric layer opposite the ferroelectric layer. The ferroelectric emitter of the present invention guarantees uniform electron emission from wide and narrow gaps of a mask layer and in an isolated pattern such as a doughnut shape for ferroelectric switching emission lithography.

FIG.1



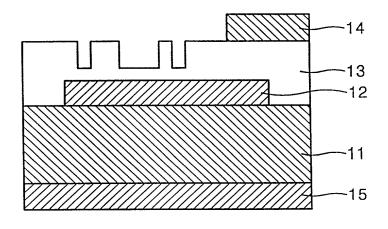


FIG.2A

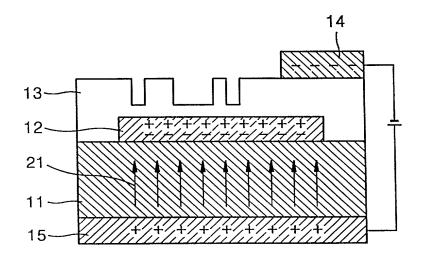


FIG.2B

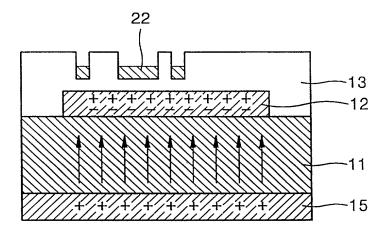


FIG.2C

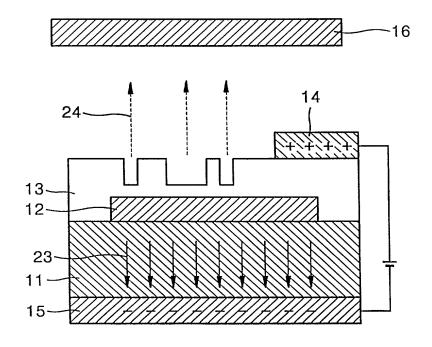


FIG.3A

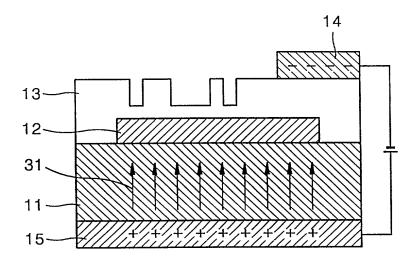


FIG.3B

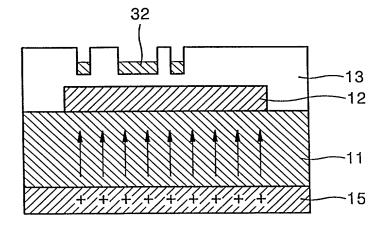


FIG.3C

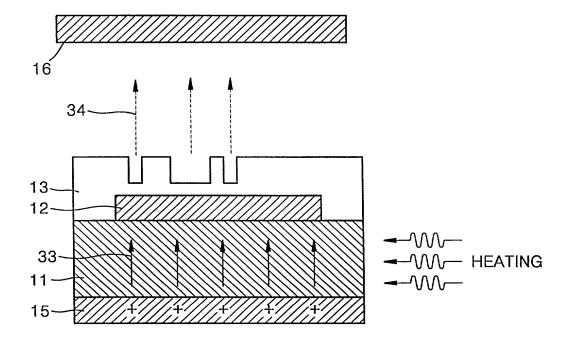
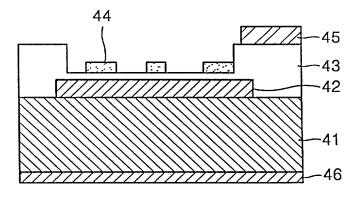


FIG. 4



DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, pust office address and citizenship are as stated below next to my name.

t believe I am the original, first and sole in below) of the subject matter which is claim FERROLLECTRIC EMITS) or an original, in the invention (first and joint inventor (if pl entitled:	nisj uatuna arc listo
the opecification of which is strached here	to unless the following box is checken	1:		
was filed on	as United States App	lication Number	or PCT International Appli	carinn Number
I hereby state that I have reviewed and it				es amended by an
I acknowledge the duty to disclose infor Regulations § 1.56.				
I hereby claim foreign priority banalita u inventur's certificate, or § 365(a) of any PC and have also identified below any foreign that of the application on which priority is PRIOR FOREIGN APPLICATION(9)				
NUMBER	COUNTRY	DA	MONTHMEAR FILED	PRIORITY CLAIMED
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I hereby claim the benefit under Title 35,	United States Code § 119(e) of any Ur	sited States prov	isional application(s) listed i	pelow.
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I hereby claim the benefit under Title 35, application designating the United States, if the prior United States for PCT Internation perhaps the prior United States for PCT Internation perhaps the grant of the perhaps the	United States Code. § 120 of any United States Code. § 120 of any United below and, insofter as the subject and application in the manner provider as the subject is known by me to be manner to be more than the prior ap	nited States applinates of each of the first parties to patent parties to patent plication and the	ication(s), or \$ 365(s) of an the claims of this application agraph of Title 35, United S willity as defined in Titls 1 national or PCT Internation	y PCT Internationa in is not disclassed is intos Codo, § 12, 17, Code of Podera tal filing date of thi
Application Serial No.	FILING DATE		STATUS: PATENTEL	PENDING.

I hereby appoint as my anomeys, with full powers of substitution and revocation, to prosecute this application and transact all business in the Patent and Tradethark Office connected therewith: Lawrence Harbin, Rog. No. 27,644; Bradford B. Kile, Rog. No. 25,223; Eugene M. Lee, Rog. No. 32,039.

Address all correspondence to Eugene M. Lee, KILE, MCINTYRE, HARBIN & LEE, The Evening Star Building Suite 500, 1101 Pennsylvania Avenue, N.W., Washington, D.C. 20004. Address all telephone communications to Eugene M. Lee. at (202) 639-1260.

I hereby doclare that all statements made herein of my nun knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or built, under Scotion 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application of any patent issued thereon.

Singapore of First or Sole Inventor.

Date

Full Name of First or Sole Invariant In-Kyeung YOO Signate	uce of First or Sole Inventor	Date 19/09/20
Residence Address olo Samsung Advanced Institute of Technology San 14-1 Nongseo-ri, Kilieung-aub, Yongin-city, Kyungki-do, Republic of Korea	Country of Cirizensh Republic of Kore	iip ea
Post Office Address Same as above		